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RESIZING AND RESHAPING OF THE NOTHING ON INSULATOR NOI TRANSISTOR

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Abstract

The paper presents some advances of a vacuum nano-transistor, known as Nothing On Insulator NOI device. The breakdown limitations are considered for ultra-thin buried oxide and different semiconductor islands shape. The relationship between oxide / semiconductor thickness and the breakdown voltage of the structure allow the gate limit voltage increasing from -6.5V to -12V using 15nm instead 10nm buried oxide. Reshaping the NOI transistor, a special semiconductor wall with one cube of roughnesses is analysed. The 1-cube variant has intermediate performances, as the maximum current capabilities.

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1. Introduction

The last years, the tunneling vacuum electron devices has known a real revival [1-5], especially based on Silicon On Insulator SOI structures [6], SOI with nano-cavity, or pure nanostructures [7]. Other times, the vacuum electronic devices adhere to alternative materials, like SiC, nano-diamond or CNT, for special applications, [8]. The combination among SOI / MOS or vacuum nano-devices opens new bridges for alternative more integrate functions, [9]. In this context, since 2005, the Nothing On Insulator NOI transistor was time to time studied and improved in its electrical static characteristics [10-13].

Its diary begun from a Silicon On Insulator SOI-MISFET transistor [14], followed by a nano-cavity [15], followed by special shaped Si-films [16]. At this stage, a thin Si-film, t_F<10nm still links the source and drain islands Fig. 1. After a complete removal of this middle film, the conduction region between source and drain rests a "Nothing On Insulator" (NOI) space - as the main body of the transistor, [10]. The conduction physical mechanisms were systematically investigated and proved to be based on the vacuum tunneling between two semiconductor islands, [17].

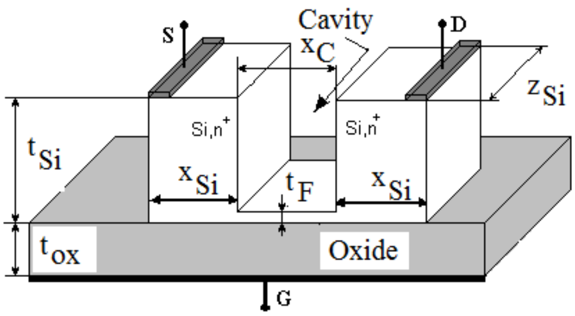

Fig. 1. The NOI device basic architecture.

Still are some un-solved items. A previous work proved a better gate control for a thinner beneath insulator, [18]. A ultra-thin insulator support offers a better drain current sensitivity, but promotes the disadvantageous substrate tunneling. Therefore, in this paper, a trade-off for the NOI nano-transistor is considered for the useful and non-useful tunneling phenomena. As additional objective of this paper, different sizes and shapes of the semiconductor layers are considered for the drain / source islands. The comparative data of the simulated NOI structures and relationship with other electronic devices are discussed in the final part of the paper, versus alternative data from the specialty literature.

3. Limitations of the gate breakdown

3.1. The buried oxide breakdown

For the NOI nanotransistor, the limits of its workframe are imposed by the beneath insulator breakdown, as emphasized few years ago, [12].

The device must resist at any failure conditions: (1) critical field in insulator; (2) negligible gate current [13]. To simulate the first situation, the following virtual experiment is created: the electric field distribution is monitored for the NOI nanotransistor biased at V_S=0V, V_D=+5V and variable V_G, till the critical electric field in oxide is reached.

In a first stage, the NOI-10nm device with 10nm Si-islands thicknesses, $N_D=10^{20}cm^{-3}$, is studied. When the critical electric field occurs in the beneath oxide, a specific parameter is defined as the limit gate voltage, $V_{G,lim}$ as V_G | $E_{cr\text{-}oxide}$ touches the bottom of the buried oxide. The simulations starts with the electric field distribution in the studied NOI device at V_S=0V, V_D=5V and V_G=-1V, fig. 2. The color code that fills the NOI nanostructure indicates that the useful tunneling occurs for a maximum electric field of 5.43×10^6V/cm in vacuum, fig. 2. The critical field $E_{cr\text{-}oxide}=1.1\times10^7$V/cm isn't still exceeded in oxide, neither at V_G=-0.5V, neither at V_G=-1V. The maximum potential drop occurs between the drain (+*5*V) and gate (-*1*V...-*n*V). In the inset from fig. 2, the electric field is cropped from a vertical cross section between drain and gate, while the drain voltage rests +5V and the gate voltage decreases step by step from -0.5V up to -9V. The incipient breakdown begins for $|V_G|$>1.6V, when $E_{cr\text{-}oxide}$ is reached in the oxide surface. Fortunately, this phenomenon takes place near the "Nothing" region and the generated carriers are captured in the source-drain current. For $|V_G|$>6.5V the electric field overcomes the critical value in the entire oxide, including the bottom of the buried oxide, producing a sure nanotransistor breakdown. So, the limit voltage on the gate, $V_{G,lim}$ = -6.5V for this NOI-10nm device. For stronger gate voltages, the entire oxide is susceptible for breakdown. In the next paragraph, some optimization solutions are searched.

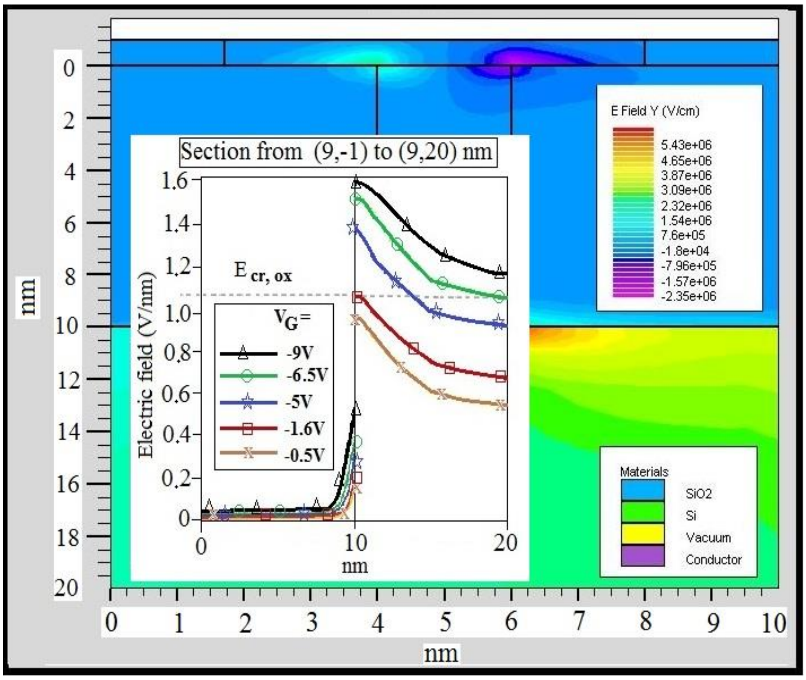

Fig. 2. The electric field distribution in the color code for the NOI-10nm device biased at V_S=0V, V_D=+5V and V_G=-1V; inset graphics for different V_G.

3.2. The NOI structure re-sizing

In order to increase the breakdown capabilities, both the oxide thickness and the semiconductor thickness are increased from 10nm to 15nm, taking into account the relationship breakdown voltage – material thickness – electric field. Also the doping concentration is increased from $10^{20}cm^{-3}$ to $N_D=7x10^{20}cm^{-3}$, accordingly with previous predictions [12], but connected to a real technology limitation, [18]. In this case, the $V_{G,lim}$ relax to -12V for our NOI-15nm device, fig. 3. The work methodology consists in the gate voltage increasing from -5V to -15V, searching the electrical field value at the interface Si-oxide, after successive simulations, fig. 3, inset.

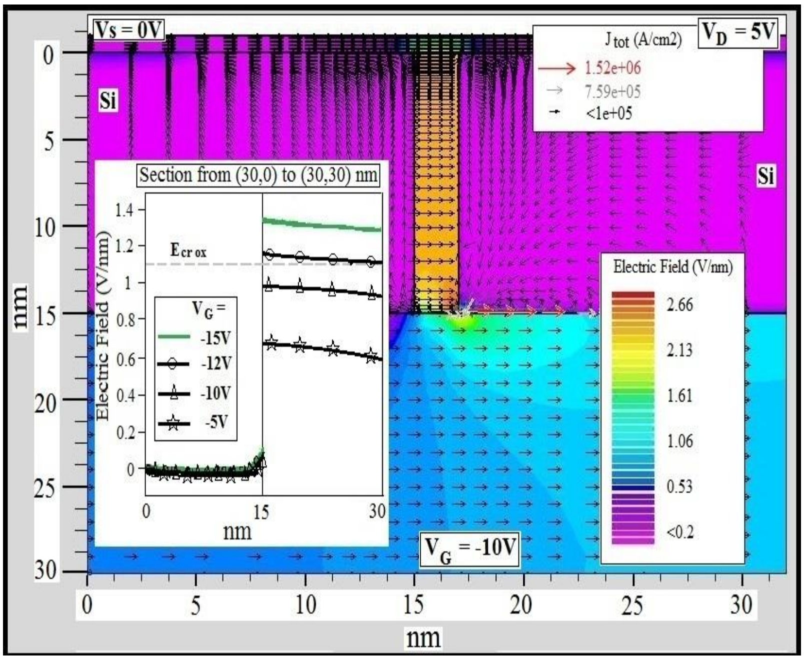

Fig. 3. The electric field distribution and current vectors for the NOI-15nm device at V_S=0V, V_D=+5V, V_G=-10V; different V_G in the inset box.

4. Reshaping the NOI-1-cube nanotransistor

In this paragraph, some rectangular growths with 0.5nm x 1nm on the vertical walls, usually released from technology [18], are simply named cubes. The last NOI structure with y_{n+} = y_{ox} = 15nm receive one pair of cubes, superior placed on the walls, fig. 4, noted by NOI-1-cube.

Also, the presence of cubes can be assimilated with the surface roughnesses [13].

In fig. 4, a magnified cross section of the NOI-1-cube device is presented at: V_S=0V, V_G=-3V and V_D =+12V. This device presents an electric field more than 1.22V/nm for 15nm<y<19nm, toward the buried oxide surface, fig. 4. However, the number of cubes doesn't influence the breakdown in the oxide. Hence, for the technological costs minimization, the 1-cube structure will be considered forward, instead old 3-cubes more expensive technique [13].

Figure 5 comparatively presents the static characteristics at V_G=-3V and V_D of different values, for simple flat NOI-15nm structures and NOI-1-cube structures. Obviously, the thinner NOI structure provides more sensitive drain current performances, but higher gate leakage currents.

Rather the drain voltage increasing pushes the transconductance to higher values, fig. 5.

5. Discussions

An oxide or semiconductor thickness increasing avoids the non-useful tunneling, but strongly alleviates the sensitivity indexed by the transconductance of the devices. However, the maximum transconductance of 0.35μA/V is offered by the flat NOI-15nm device biased at

V_{DS}=7V, fig. 5, being superior in range as for a classical vacuum fabricated device when $V_G \rightarrow 0$V, [19] and in a close range as for a more recent vacuum nanotransistor [20]. The other NOI transconductances almost vanish, especially for a drain voltage under the threshold value, [18]. Neither the cubes presence, neither the semiconductor material improved the NOI-15nm transconductance. It is expected that Germanium On Insulator structures offer a better impact of the modulated subthreshold characteristics, by quantum confinement on the back-gate bias [21]. The GeOI devices exhibit higher sensitivity than the SOI counterpart due to its smaller quantization effective mass.

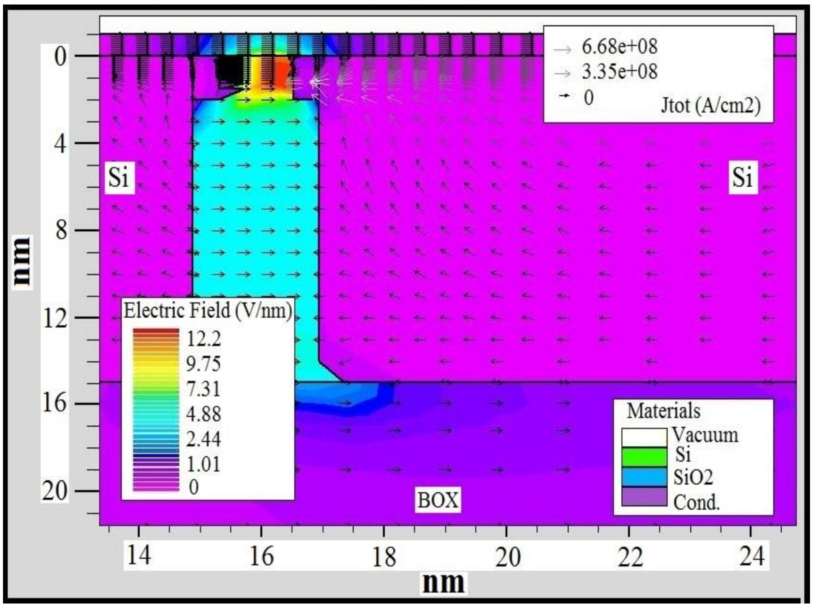

Fig. 4. The electric field distribution and the current density vectors at V_G=-3V, V_D =+12V for devices with 15nm semiconductor film on 15nm oxide: Si-NOI with 1 cube.

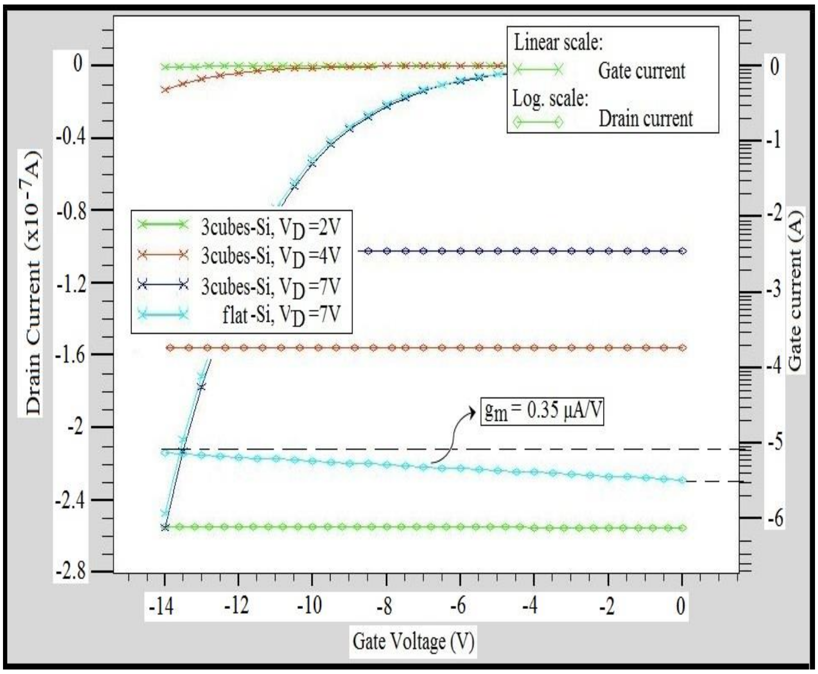

Fig. 5. The curves I_D-V_G (log at right side) and I_G-V_G (linear at left side) at V_{DS}=2, 4, 7V, for Si-NOI-15nm 1-cube with N_D=7x10^{20}cm^{-3}.

The NOI-1-cube variant offers superior I_D and I_G performances than the NOI-15nm or NOI-10nm similar variants, associated with poorer transconductance, in the same voltages range.

An immediate application concerns the sensors that need few nano-amperes currents transformation into few volts on the gate, at a given drain-source voltage, [22].

The NOI frequent applications go to the semiconductor-vacuum emission transistors [23]. By this study, the NOI devices approaches to the recent nano-transistors with vacuum, which usually suffer from large area consuming and posses typical transconductances of 1÷10μA/V.

In further applications, the NOI device can act as active device: vacuum nano-diode [18] or in switching applications [13] when it is acted by a sole V_{DS} voltage at a constant V_{GS} or a vacuum nano-transistor acted by both V_{DS} and V_{GS} in a similar manner as another device class has grown in the last years, [20, 23].

6. Conclusions

This paper studied the Nothing On Insulator nanotransistor with different sizes and shapes. A quantitative breakdown limitation was established by a sole parameter: $V_{G,lim}$ in order to avoid the critical electric field reaching in the entire buried oxide. In a first stage, the limit gate voltage, $V_{G,lim}$ was defined as that gate voltage that produces an critical electrical field deep into the beneath oxide till the bottom of the oxide. The NOI-10nm structure gets -6.5V for this parameter. In a second stage, the oxide and semiconductor films increased their thicknesses from 10nm up to 15nm to increase the breakdown capabilities. In the last stage, the NOI device get one pair of cube on the semiconductor surface, as a usual effect of roughnesses. In this case, the drain current increases versus the flat surface NOI device, but accompanied by a poorer transconductance.

The practical usefulness of NOI device comes from its operation parameters: high capability in drain current device, low area consumption in nano-metric range, commanded by lower gate voltages as usual vacuum devices.

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